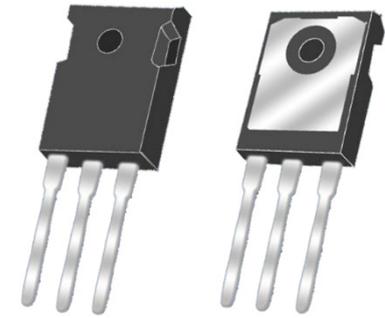


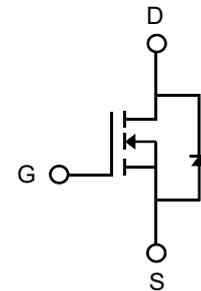
## Description

The PSMTAF10R2H uses split gate trench technology to provide excellent  $R_{DS(ON)}$  low gate charge. This device is suitable for power management and high efficiency applications at high switching frequencies applications.



G D S

TO-247-3L



Circuit Diagram



Marking (Top View)

MOSFET Product Summary		
$V_{DS}(V)$	$R_{DS(on)}(m\Omega)$	$I_D(A)$
100	2.1@ $V_{GS} = 10V$	300

## Feature

- Low  $R_{DS(ON)}$  - Ensures On-State Losses are Minimized
- Excellent  $Q_{gd} \times R_{DS(ON)}$  Product(FOM)
- Advanced Technology for DC-DC Converts
- Small Form Factor Thermally Efficient Package  
Enables Higher Density End Products
- 100% UIS (Avalanche) Rated
- Lead-Free Finish ; RoHS Compliant
- Halogen and Antimony Free. "Green" Device

## Applications

- PWM applications
- Load switch
- Power management
- DC-DC Converters
- Wireless Chargers

## Absolute maximum rating@25°C

Rating	Symbol	Value	Units
Drain-Source Voltage	$V_{DS}$	100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous <sup>1)</sup>	$I_D$	$T_C=25^\circ C$	300
		$T_C=100^\circ C$	197
Pulsed Drain Current <sup>2)</sup>	$I_{DM}$	1200	A
Total Power Dissipation <sup>3)</sup>	$P_D$	390.6	W
Avalanche Current <sup>4)</sup>	$I_{AS}$	122	A
Avalanche Energy <sup>4)</sup>	$E_{AS}$	2231	mJ
Thermal Resistance , Junction-case <sup>5)</sup>	$R_{\theta JC}$	0.32	$^\circ C/W$
Thermal Resistance Junction-to-Ambient <sup>6)</sup>	$R_{\theta JA}$	29.67	$^\circ C/W$
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55~+150	$^\circ C$

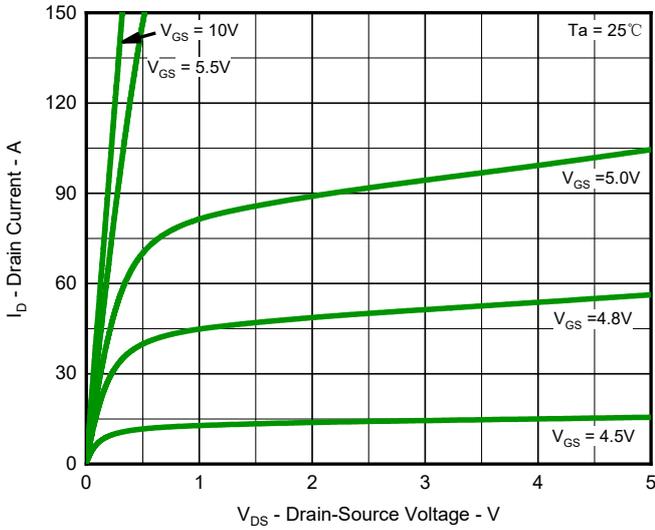
## Electrical characteristics per line@25°C (unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	100	110	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 100V, V_{GS} = 0V$	-	-	1.0	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS} = \pm 20V, V_{DS} = 0V$	-	-	$\pm 100$	nA
<b>On Characteristics</b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	2.2	3.3	3.8	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 50A$	-	2.1	2.6	m $\Omega$
<b>Dynamic Characteristics<sup>7)</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 50V, V_{GS} = 0V,$ $f = 1.0MHz$	-	11100	-	pF
Output Capacitance	$C_{oss}$		-	1860	-	
Reverse Transfer Capacitance	$C_{rss}$		-	31	-	
<b>Switching Characteristics<sup>7)</sup></b>						
Turn-on Delay Time	$t_{d(on)}$	$V_{DS} = 50V, V_{GS} = 10V,$ $R_G = 10\Omega, I_D = 50A$	-	99.9	-	ns
Turn-on Rise Time	$t_r$		-	95.8	-	
Turn-Off Delay Time	$t_{d(off)}$		-	195.8	-	
Turn-Off Fall Time	$t_f$		-	88.6	-	
Total Gate Charge	$Q_g$	$V_{DS} = 50V, V_{GS} = 10V,$ $I_D = 50A$	-	169	-	nC
Gate-Source Charge	$Q_{gs}$		-	69.1	-	
Gate-Drain Charge	$Q_{gd}$		-	38.8	-	
Gate Resistance	$R_g$	f=1MHz, Open Drain	-	2.6	-	$\Omega$
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage	$V_{SD}$	$V_{GS} = 0V, I_S = 1A$	-	0.7	1.3	V

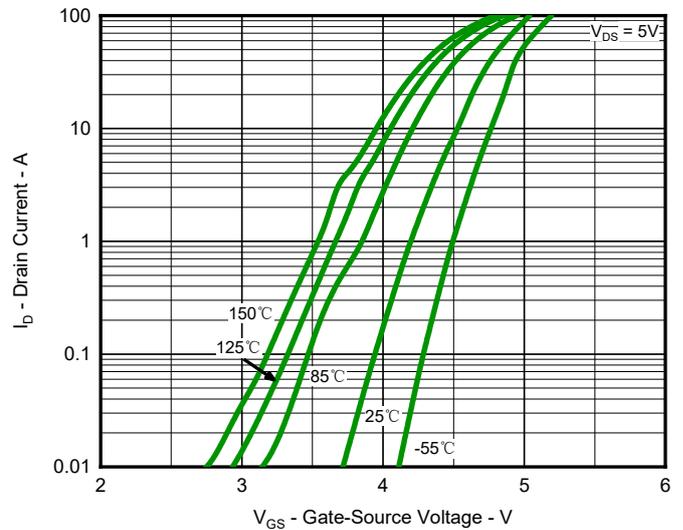
## Notes:

1. Computed continuous current assumes the condition of  $T_{J\_Max}$  while the actual continuous current depends on the thermal & electro-mechanical application board design.
2. Repetitive Rating: Pulse width limited by maximum junction temperature( $T_{J\_Max}=150^\circ C$ ).
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. This single-pulse measurement was taken under the following condition [ $L=300\mu H, V_{GS}=10V, V_{DS}=100V$ ]while it's value is limited by  $T_{J\_Max}=150^\circ C$
5. Device mounted on infinite heatsink
6. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
7. Guaranteed by design, not subject to production

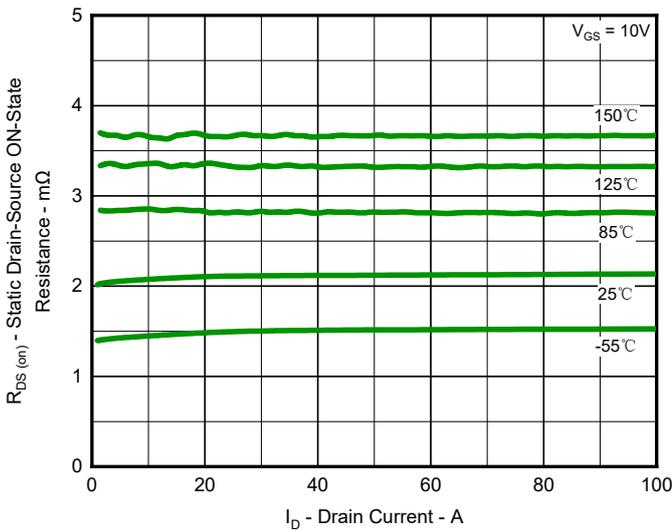
## Typical Characteristics



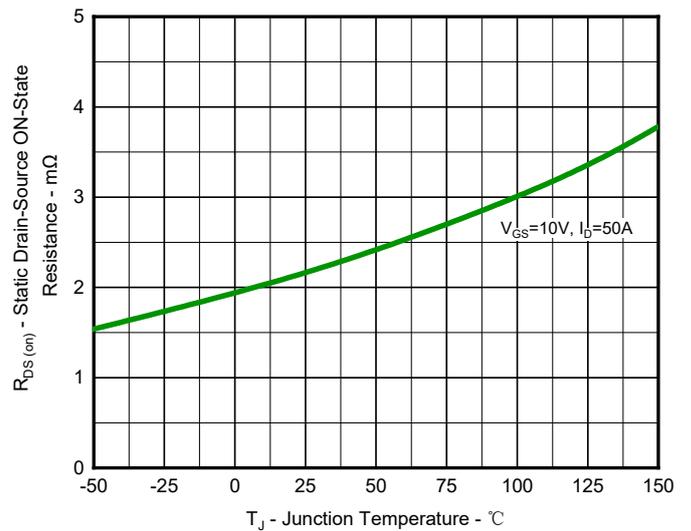
**Fig.1 Output Characteristics**



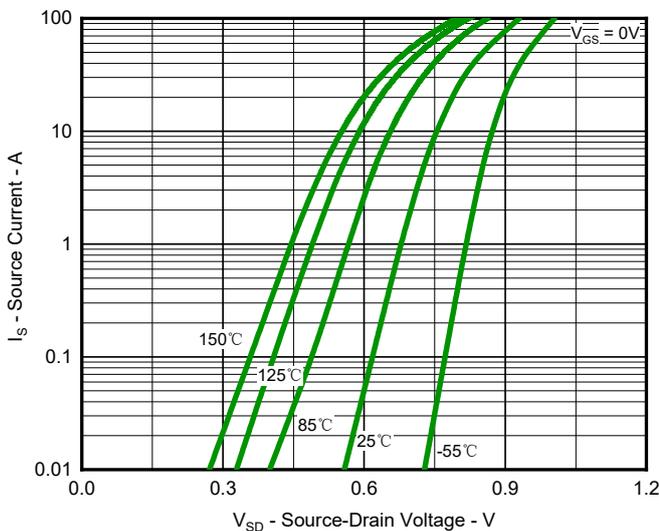
**Fig.2 Typical Transfer Characteristic**



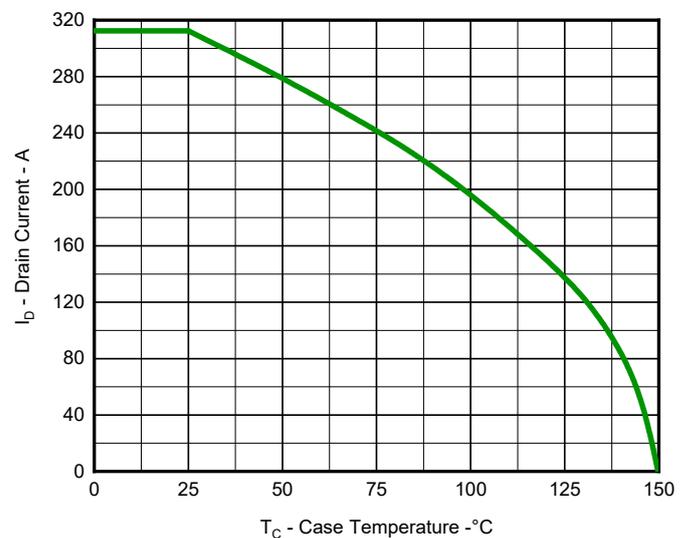
**Fig.3 Typical On-Resistance vs Drain Current and Temperature**



**Fig.4 On-Resistance Variation with Temperature**



**Fig.5 Diode Forward Voltage vs. Current**



**Fig.6 Maximum Drain Current vs. Case Temperature**

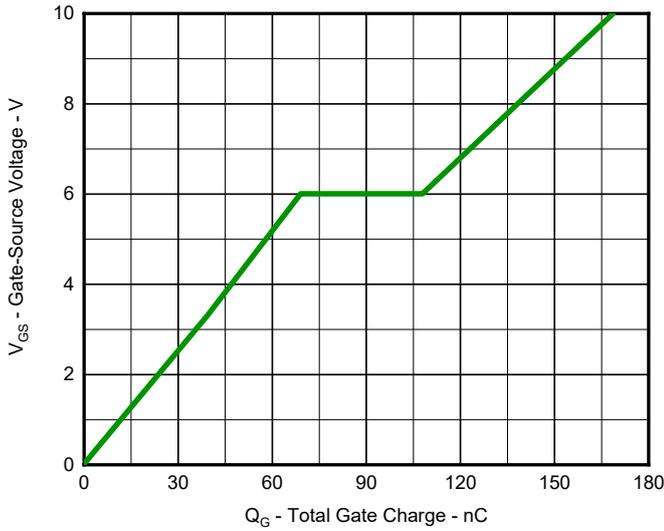


Fig.7 Gate Charge Characteristics

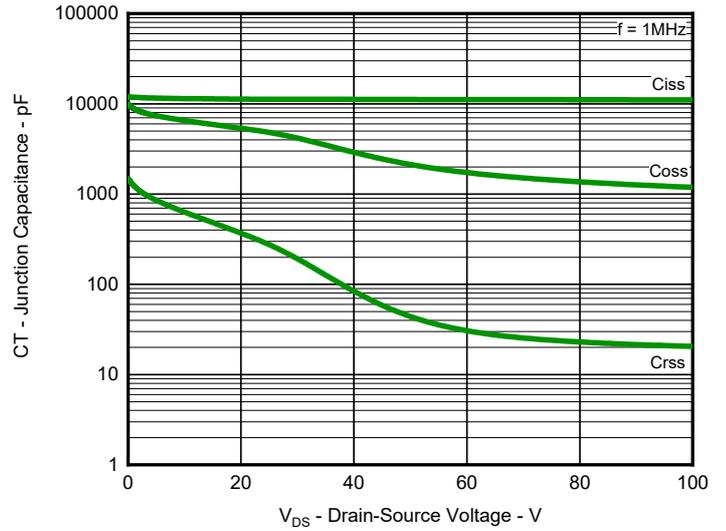


Fig.8 Typical Junction Capacitance

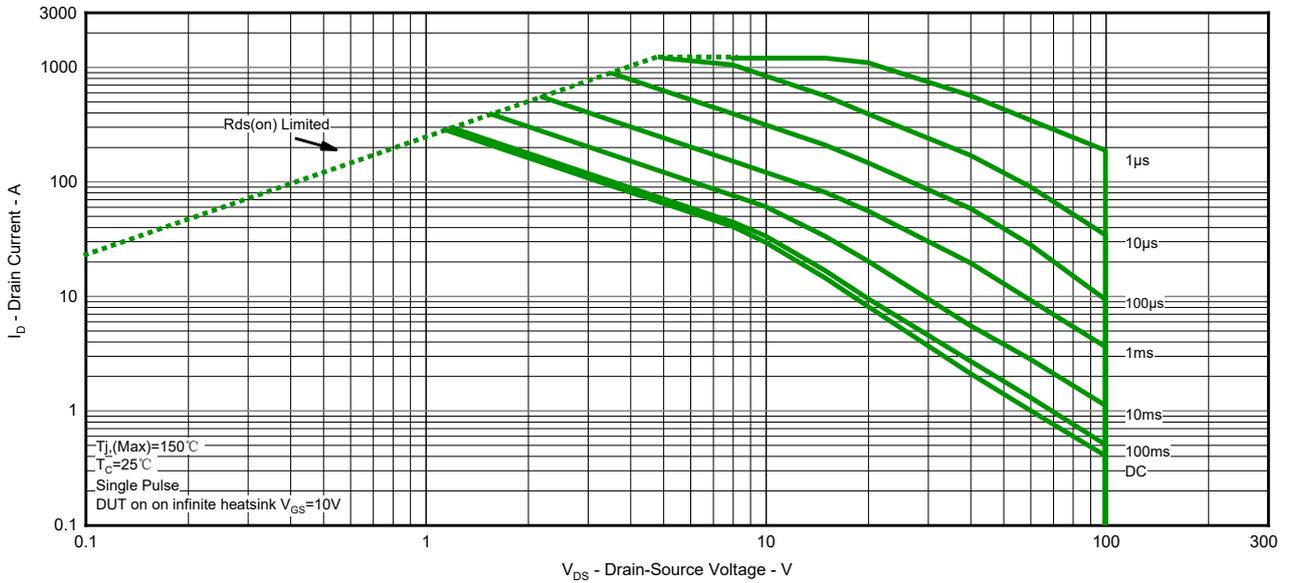


Fig.9 Safe Operation Area

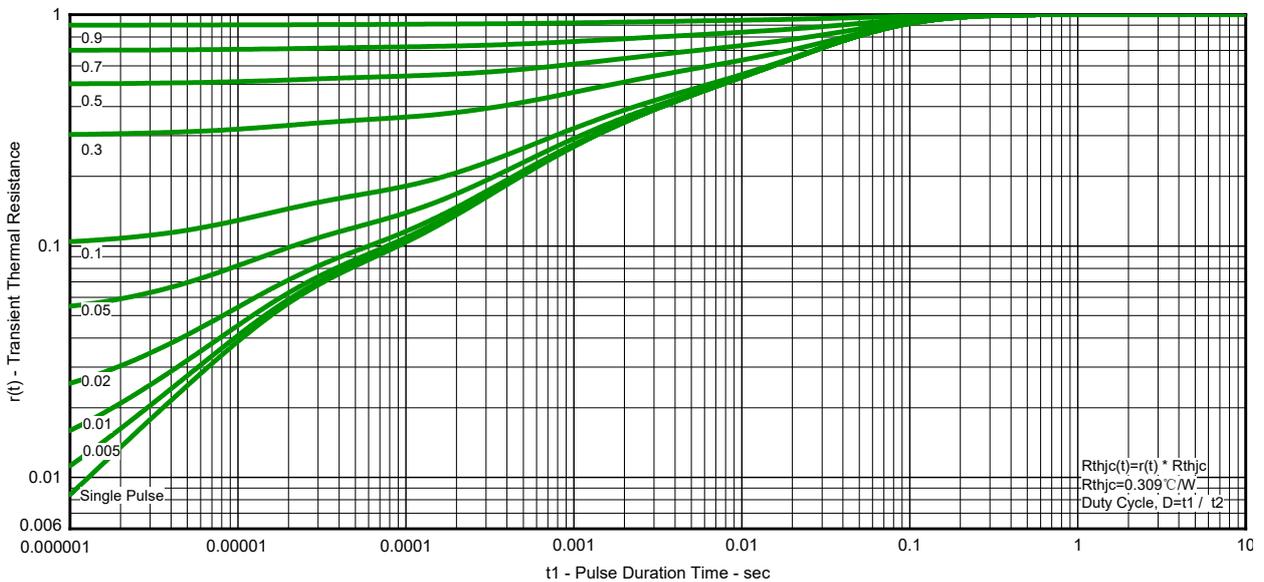
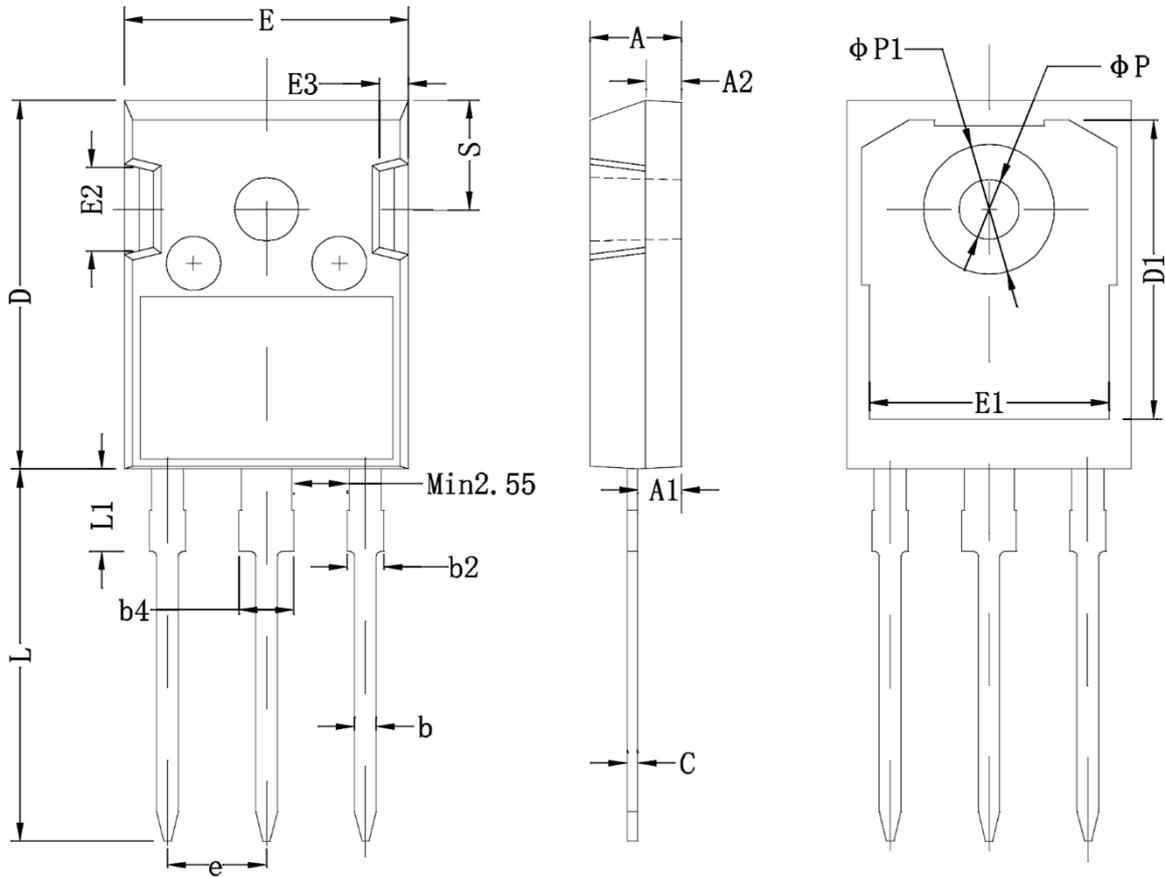


Fig.10 Transient Thermal Resistance

Product Dimension (TO-247-3L)



Dim	Millimeters		Inches		Dim	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	4.80	5.20	0.189	0.205	E1	13.00	13.60	0.512	0.535
A1	2.21	2.59	0.087	0.102	E2	4.80	5.20	0.189	0.205
A2	1.85	2.15	0.073	0.085	E3	2.30	2.70	0.091	0.106
b	1.11	1.36	0.044	0.054	e	5.44 BSC.		0.214 BSC.	
b2	1.91	2.21	0.075	0.087	L	19.82	20.22	0.780	0.796
b4	2.91	3.21	0.115	0.126	L1	-	4.30	-	0.169
c	0.51	0.75	0.020	0.030	φP	3.40	3.80	0.134	0.150
D	20.80	21.30	0.819	0.839	φP1	-	7.30	-	0.287
D1	16.25	16.85	0.640	0.663	S	6.15 BSC.		0.242 BSC.	
E	15.50	16.10	0.610	0.634					

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