

## Description

The PSMTL10R2 uses split gate trench technology to provide excellent  $R_{DS(ON)}$  and low gate charge. This device is suitable for power management and high efficiency applications at high switching frequencies applications.

### MOSFET Product Summary

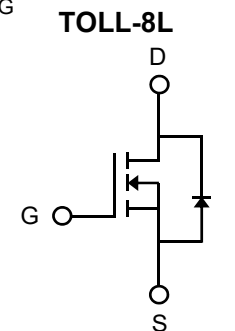
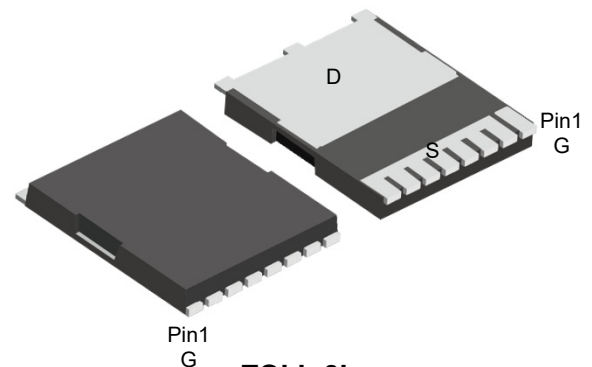
$V_{DS}(V)$	$R_{DS(on)}(m\Omega)(Typ)$	$I_D(A)$
100	1.4@ $V_{GS} = 10V$	351

## Feature

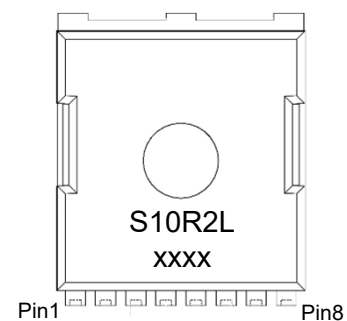
- Low  $R_{DS(ON)}$  - Ensures On-State Losses are Minimized
- Excellent  $Q_{gd} \times R_{DS(ON)}$  Product(FOM)
- Advanced Technology for DC-DC Converts
- Small Form Factor Thermally Efficient Package  
Enables Higher Density End Products
- 100% UIS (Avalanche) Rated
- Lead-Free Finish ; RoHS Compliant
- Halogen and Antimony Free. "Green" Device

## Applications

- PWM applications
- Load switch
- Power management
- DC-DC Converters
- Wireless Chargers



**Circuit Diagram**



**Marking (Top View)**

## Absolute maximum rating@25°C

Rating		Symbol	Value	Units
Drain-Source Voltage		$V_{DS}$	100	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	V
Drain Current-Continuous <sup>1)</sup>	$T_C=25^\circ C$	$I_D$	351	A
	$T_C=100^\circ C$		249	
Pulsed Drain Current <sup>2)</sup>		$I_{DM}$	1406	A
Total Power Dissipation <sup>4)</sup>	$T_C=25^\circ C$	$P_D$	429	W
	$T_C=100^\circ C$		214	
Avalanche Current @ $L=0.3mH$		$I_{AS}$	71	A
Avalanche Energy @ $L=0.3mH$		$E_{AS}$	756	mJ
Thermal Resistance , Junction-to-Case <sup>4)</sup>		$R_{\theta JC}$	0.35	$^\circ C/W$
Thermal Resistance Junction-to-Ambient <sup>3)</sup>		$R_{\theta JA}$	29	$^\circ C/W$
Junction and Storage Temperature Range		$T_J, T_{STG}$	-55~+150	$^\circ C$

## Electrical characteristics per line@25°C (unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
Off Characteristics							
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA		100	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 100V, V <sub>GS</sub> = 0V	T <sub>J</sub> =25°C	-	-	1.0	μA
			T <sub>J</sub> =55°C	-	-	10	
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V		-	-	±100	nA
On Characteristics <sup>5)</sup>							
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA		2.0	3.0	4.0	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 20A		-	1.4	1.7	mΩ
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 20A		-	67	-	S
Diode Forward Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0V, I <sub>S</sub> = 1A		-	0.7	1.2	V
Dynamic Characteristics <sup>6)</sup>							
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 50V, V <sub>GS</sub> = 0V, f = 1.0MHz		-	9665	-	pF
Output Capacitance	C <sub>oss</sub>			-	2065	-	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	59	-	
Switching Characteristics <sup>6)</sup>							
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DS</sub> = 50V, V <sub>GS</sub> = 10V, R <sub>G</sub> = 3Ω, I <sub>D</sub> = 20A		-	21	-	ns
Turn-on Rise Time	t <sub>r</sub>			-	28	-	
Turn-Off Delay Time	t <sub>d(off)</sub>			-	72	-	
Turn-Off Fall Time	t <sub>f</sub>			-	37	-	
Total Gate Charge @ V <sub>GS</sub> = 10V	Q <sub>g</sub>	V <sub>DS</sub> = 50V, I <sub>D</sub> = 20A, V <sub>GS</sub> = 10V,		-	134	-	nC
Total Gate Charge @ V <sub>GS</sub> = 6V				-	86	-	
Gate-Source Charge	Q <sub>gs</sub>			-	36	-	
Gate-Drain Charge	Q <sub>gd</sub>			-	27	-	
Gate Resistance	R <sub>g</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz		-	1.4	-	Ω
Drain-Source Diode Characteristics <sup>6)</sup>							
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> =20A, d <sub>I</sub> /d <sub>t</sub> =100A/μs		-	85	-	ns
Reverse Recovery Charge	Q <sub>rr</sub>			-	251	-	nC
Diode Forward Current	I <sub>S</sub>	-		-	-	351	A

## Notes:

1. Pulse width limited by maximum junction temperature.
2. Pulse test : Pulse width  $\leq 100\mu s$ , duty cycle  $\leq 2\%$ .
3. Device mounted on 1 inch FR4 PCB with 2oz.Copper.
4. Device mounted on infinite heatsink.
5. Measured under pulsed conditions. Pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$ .
6. Guaranteed by design, not subject to production.

## Typical Characteristics

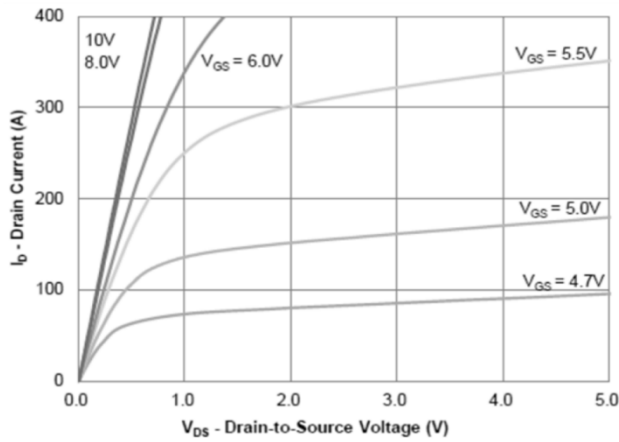


Figure 1: Output Characteristics

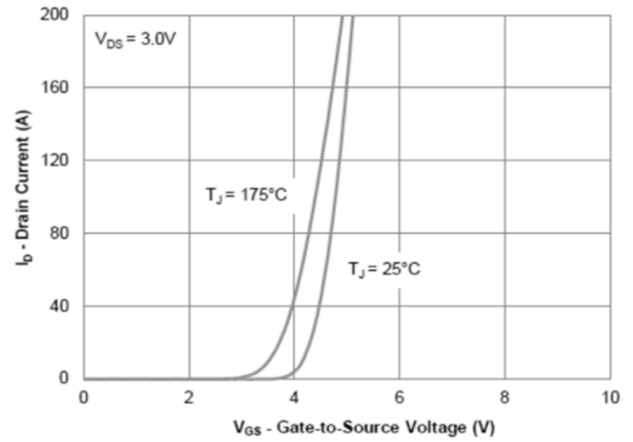


Figure 2: Transfer Characteristics

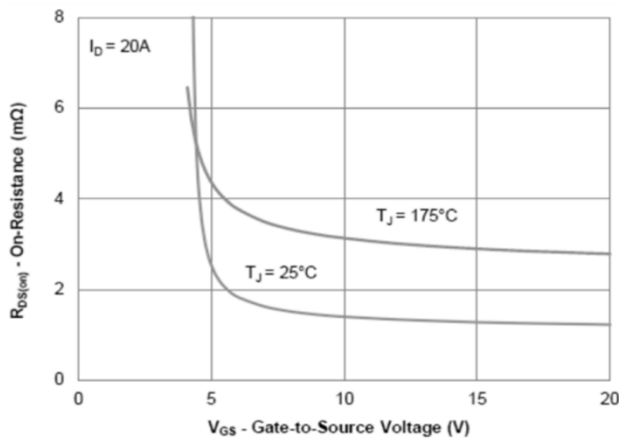


Figure 3: On-Resistance vs. Gate-Source Voltage

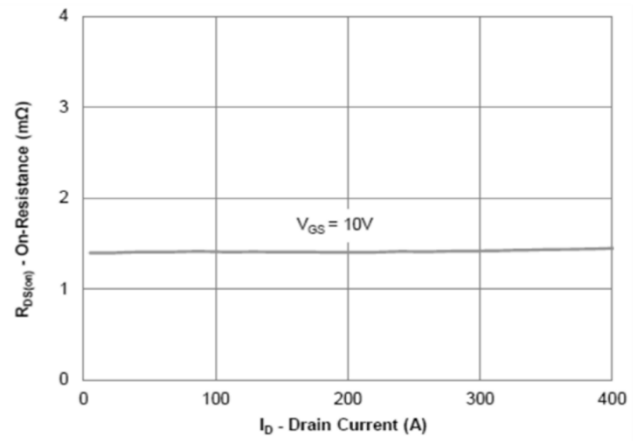


Figure 4: On-Resistance vs. Drain Current

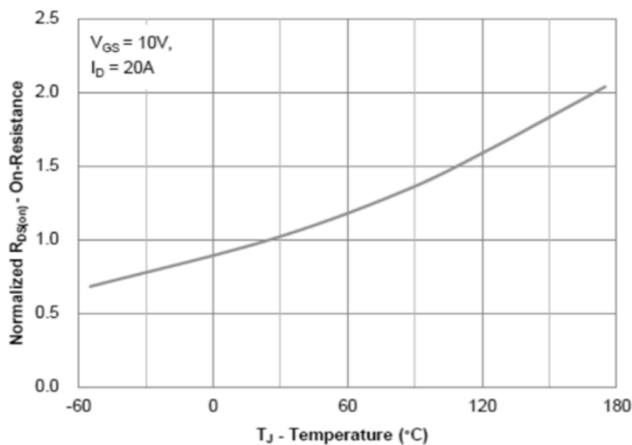


Figure 5: On-Resistance vs. Junction Temperature

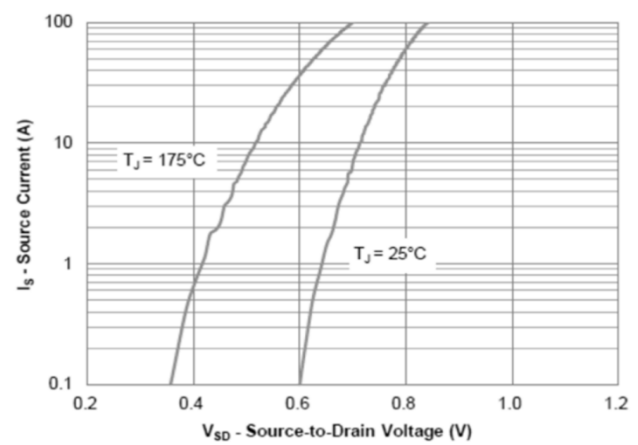


Figure 6: Source-Drain Diode Forward Voltage

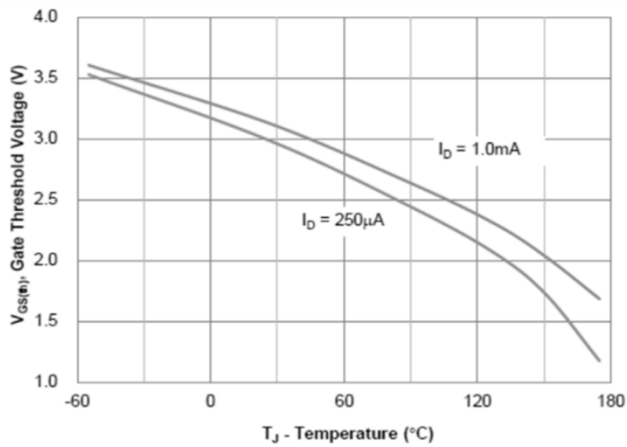


Figure 7: Gate Threshold Variation vs. Junction Temperature

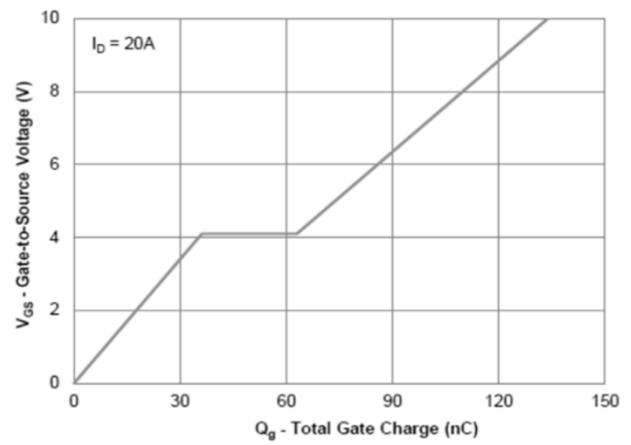


Figure 8: Gate Charge Characteristics

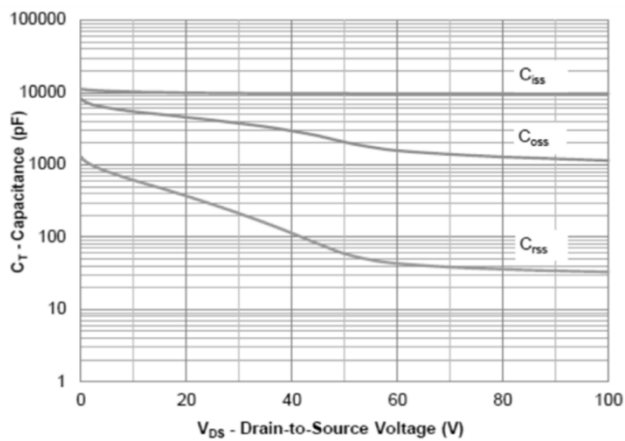


Figure 9: Capacitance Characteristics

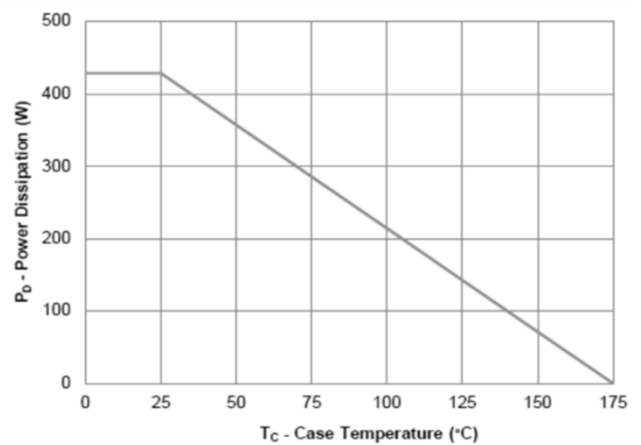


Figure 10: Power Derating

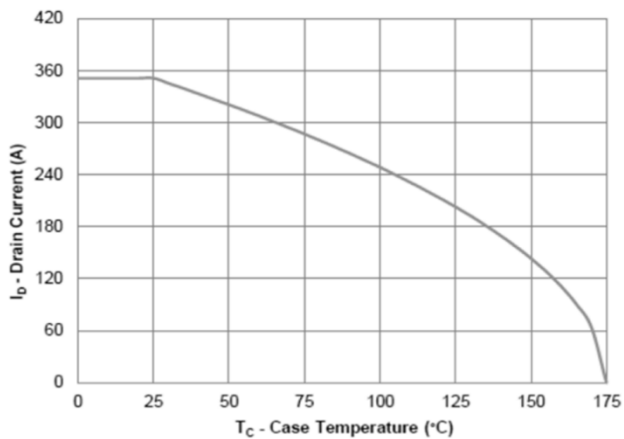


Figure 11: Current Derating

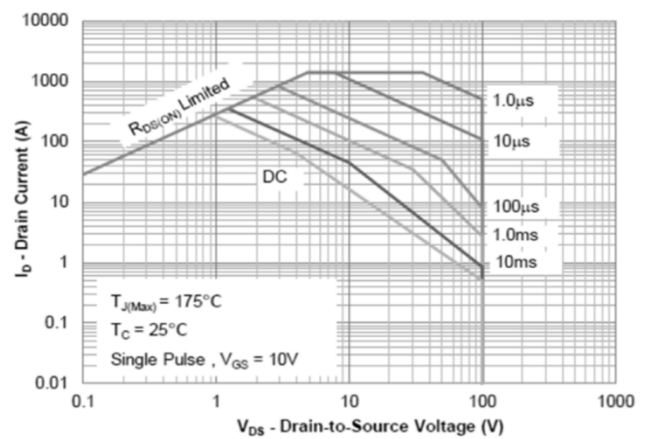


Figure 12: Safe Operating Area

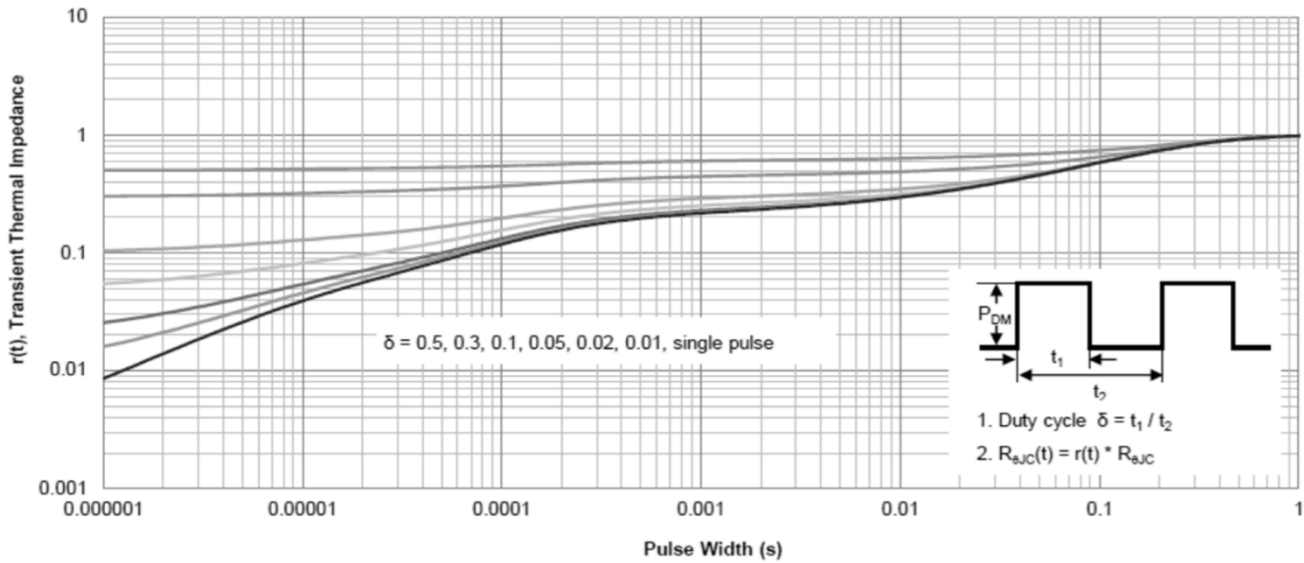
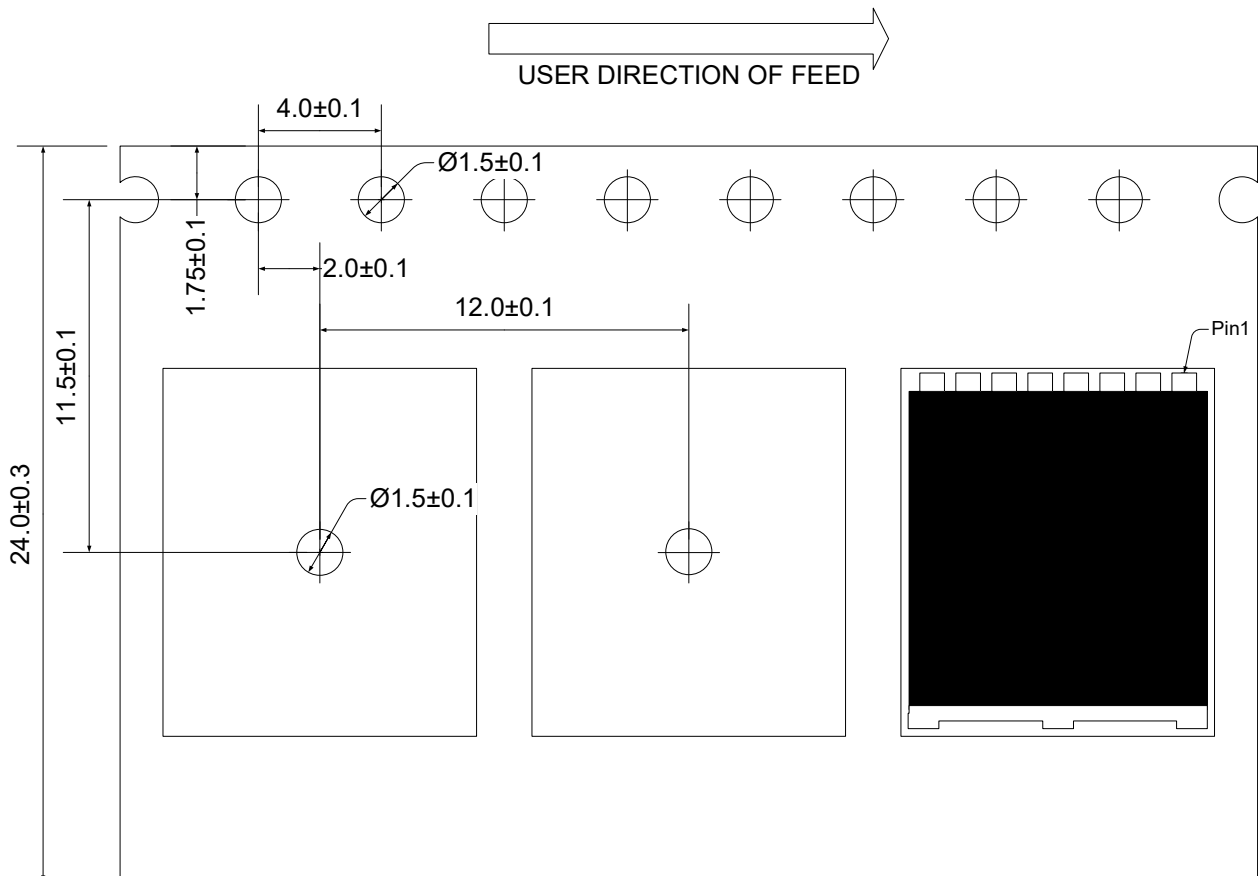


Figure 13: Normalized Maximum Transient Thermal Impedance

## Ordering Information

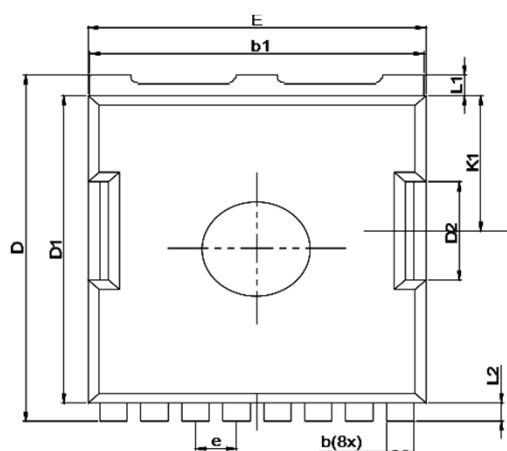
Device	Package	Reel	Shipping
PSMTL10R2	TOLL-8L	13"	2000 / Tape & Reel

## Load With Information

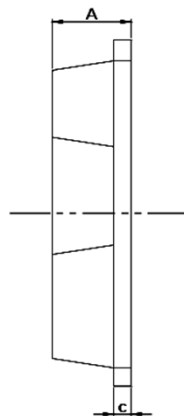


Unit:mm

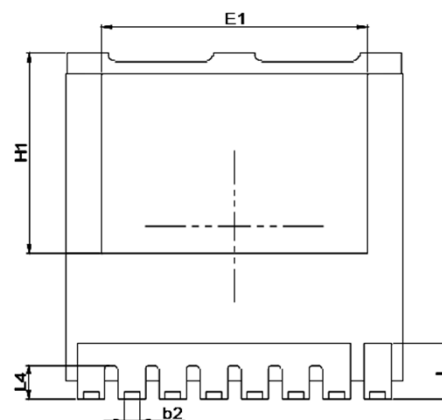
## Product Dimension (TOLL-8L)



Top View



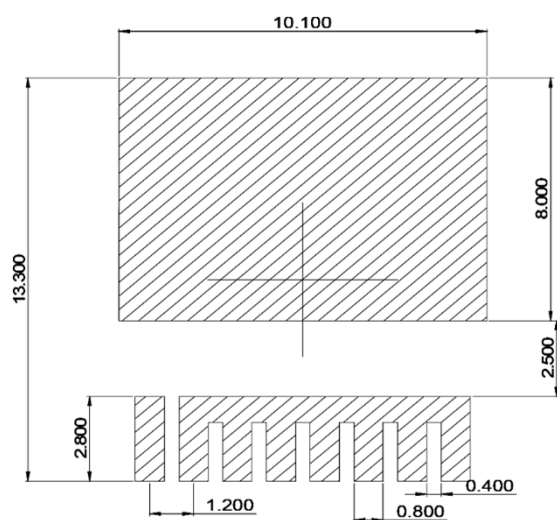
Side View



Bottom View



Front View




Unit: mm

Suggested PCB Layout

Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	2.20	2.40	0.087	0.094
b	0.65	0.90	0.026	0.035
b1	9.65	9.95	0.380	0.392
c	0.40	0.60	0.016	0.024
D	11.48	11.95	0.452	0.470
D1	10.25	10.70	0.404	0.421
D2	2.85	3.40	0.112	0.134
E	9.70	10.10	0.382	0.398
E1	8.00	9.25	0.315	0.364
e	1.20 BSC		0.047 BSC	
H1	6.70	7.30	0.264	0.287
K1	4.55 BSC		0.179 BSC	
L	1.35	2.10	0.053	0.083
L1	0.70 BSC		0.028 BSC	
L2	0.60 BSC		0.024 BSC	
L4	0.95	1.35	0.037	0.053


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